(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
14 July 2005 (14.07.2005)

PCT

(10) International Publication Number
WO 2005/062998 A2

(51) International Patent Classification: Not classified

(21) International Application Number:
PCT/US2004/044097

(22) International Filing Date:
11 December 2004 (11.12.2004)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/529,166 12 December 2003 (12.12.2003) US
60/544,702 5 December 2004 (05.12.2004) US

(71) Applicant *(for all designated States except US)*: **GREAT WALL SEMICONDUCTOR CORPORATION** [US/US]; P.O. Box 24619, Southern Avenue, Tempe, AZ 85285-4619 (US).

(72) Inventors: **ANDERSON, Samuel, S.**; 911 West Diamond Drive, Tempe, AZ 85283 (US). **SHEN, Zheng**; 3719 Savannah Loop, Oviedo, FL 32765 (US). **OKADA, David, N.**; 7855 South River Parkway, Suite 122, Tempe, AZ 85284 (US).

(74) Agents: **SAMUEL, Richard, I.** et al.; Goodwin Procter LLP, 103 Eisenhower Parkway, Roseland, NJ 07068 (US).

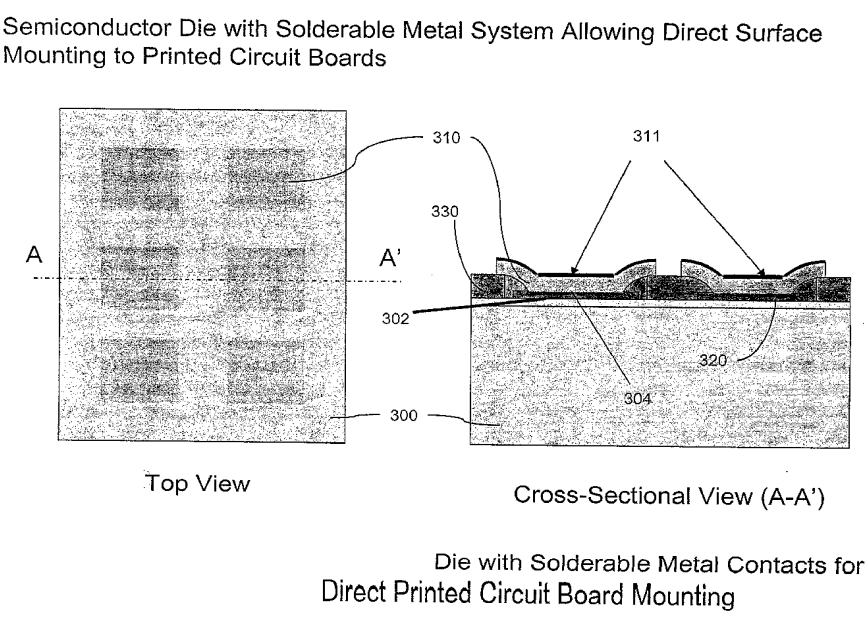
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *without international search report and to be republished upon receipt of that report*

[Continued on next page]

(54) Title: METAL INTERCONNECT SYSTEM AND METHOD FOR DIRECT DIE ATTACHMENT



(57) Abstract: Provided herein is an exemplary embodiment of a semiconductor chip for directly connecting to a carrier. The chip includes a metal layer applied to a top surface of the chip; a passivation layer applied over the metal layer such that portions of the passivation layer is selectively removed to create one or more openings ("bond pads") exposing portions of the metal layer and one or more solderable metal contact regions formed on each of the one or more openings. The solderable metal contact regions electrically connect to the carrier when the chip is positioned face down on the carrier, supplied with a thin layer of solder and heated.

WO 2005/062998 A2

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.